



TLM 2.0 Loosely Timed (LT) System Example - Simple

Jack Donovan, Anna Keist, Charles Wilson

ESLX, Inc.

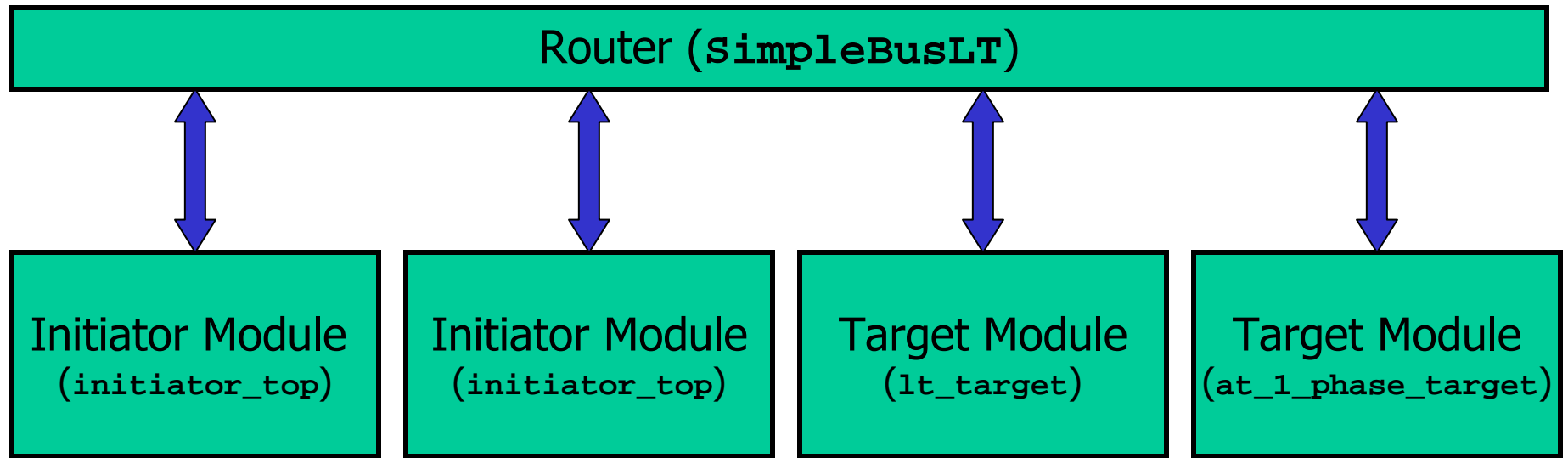
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AT System Example - Annotated Timing

- **The Goal is to Illustrate:**
 - Application of TLM 2.0 in a real system
 - Annotated non-blocking (NB) option of the non-blocking style
 - ◆ NB annotated timing has been referred to as "1 phase"
 - ◆ Simplest version of non-blocking/AT
- **Possible Applications:**
 - Architectural exploration
 - Early software development



Example Block Diagram



 TLM 2 GP

How to run this example (Linux)

- Set `SYSTEMC_HOME`
- `cd examples/tlm/lt/build-unix`
- `make clean`
- `make`
- `make run`

How to run this example (MSVC)

- Open a explorer window on `examples/tlm/lt/build-windows`
- Launch `lt.sln`
- Select '**Property Manager**' from the '**View**' menu
- Under '**lt > Debug | Win32**' select '**systemc**'
- Select '**Properties**' from the '**View**' menu
- Select '**User Macros**' under '**Common Properties**'
- Update the '**SYSTEMC**' entry and apply
- Build and run

Expected Output (expected.log)

Info: lt_initiator.cpp: 80 ns - initiator_thread
Initiator: 101 b_transport(GP, 0 s)

Info: report.cpp: 80 ns - print
ID: 201 COMMAND: WRITE Length: 04
Addr: 0x0000000000000004 Data: 0x00000004

Info: at_target_1_phase.cpp: 80 ns - b_transport
Target: 201 returned delay of 0 s + 20 ns + 60 ns = 80 ns

Info: lt_initiator.cpp: 80 ns - initiator_thread
Initiator: 101 b_transport returned delay = 80 ns

Info: lt_initiator.cpp: 80 ns - initiator_thread
Initiator: 102 b_transport(GP, 0 s)

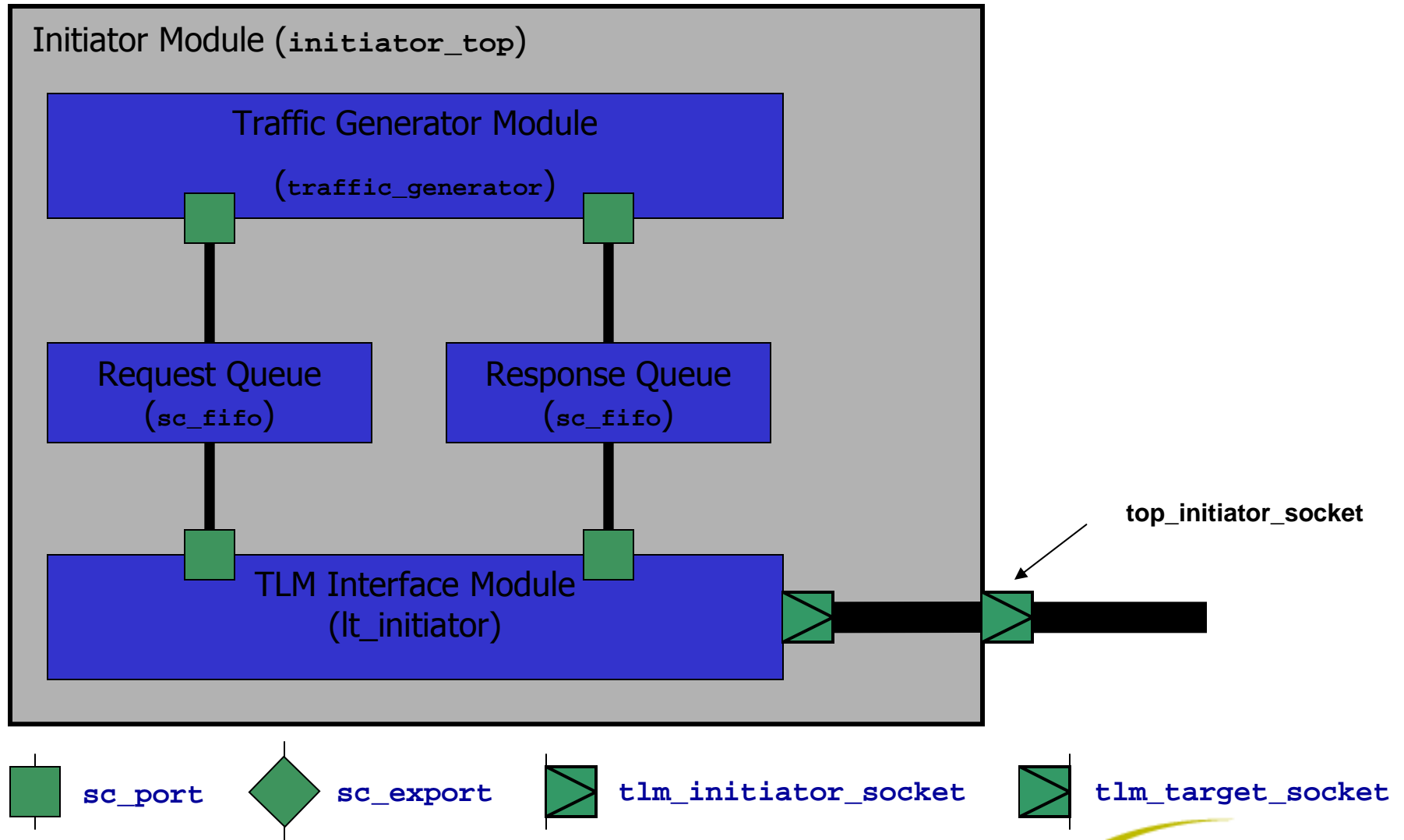
Info: report.cpp: 80 ns - print
ID: 201 COMMAND: WRITE Length: 04
Addr: 0x0000000000000004 Data: 0x00000004

Info: at_target_1_phase.cpp: 80 ns - b_transport
Target: 201 returned delay of 0 s + 20 ns + 60 ns = 80 ns

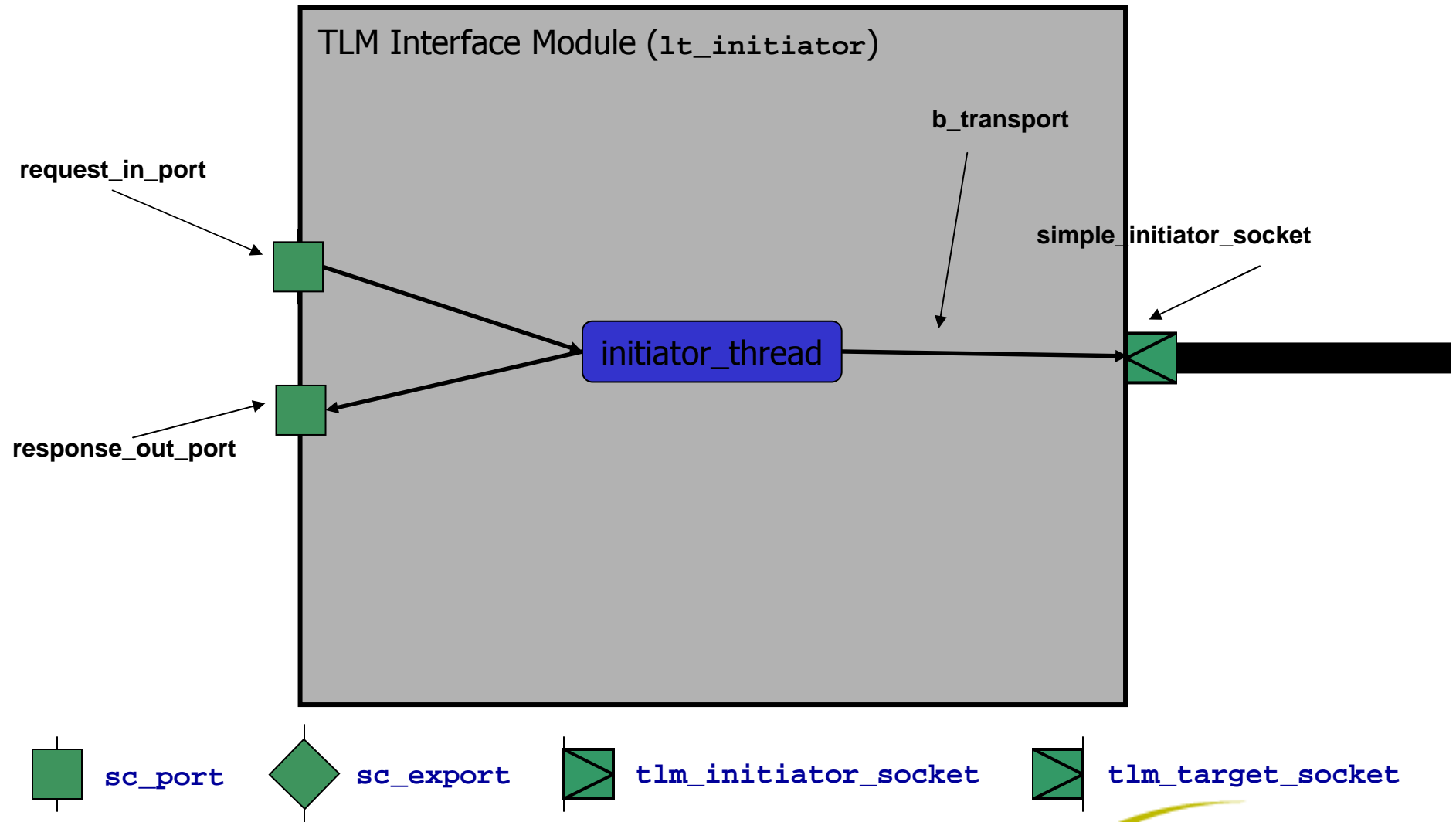
Info: lt_initiator.cpp: 80 ns - initiator_thread
Initiator: 102 b_transport returned delay = 80 ns



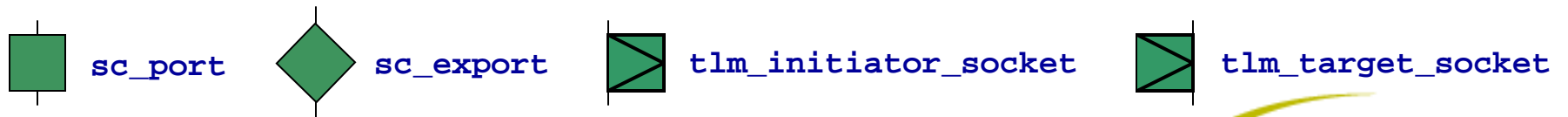
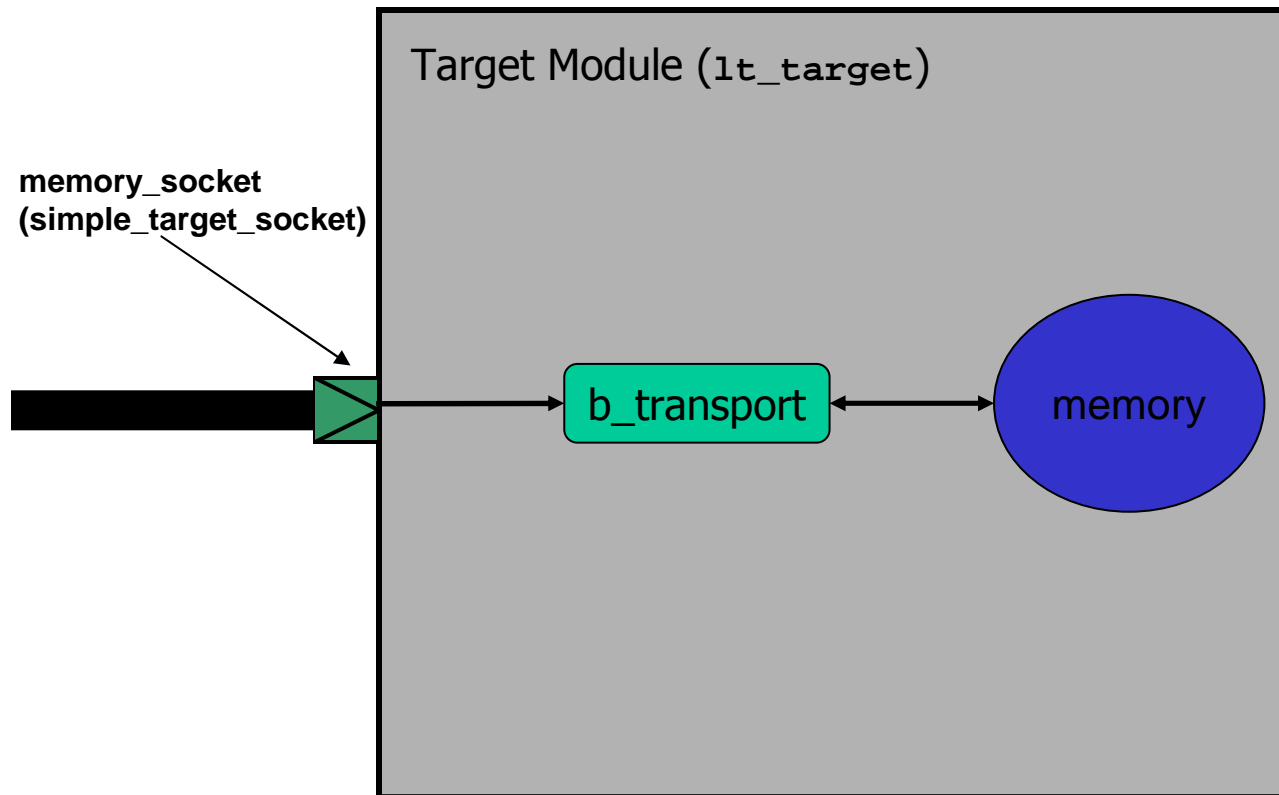
Initiator Module



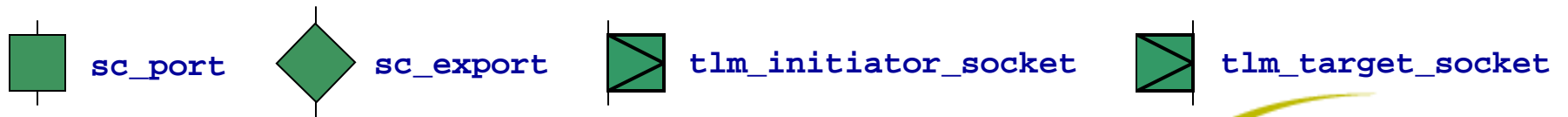
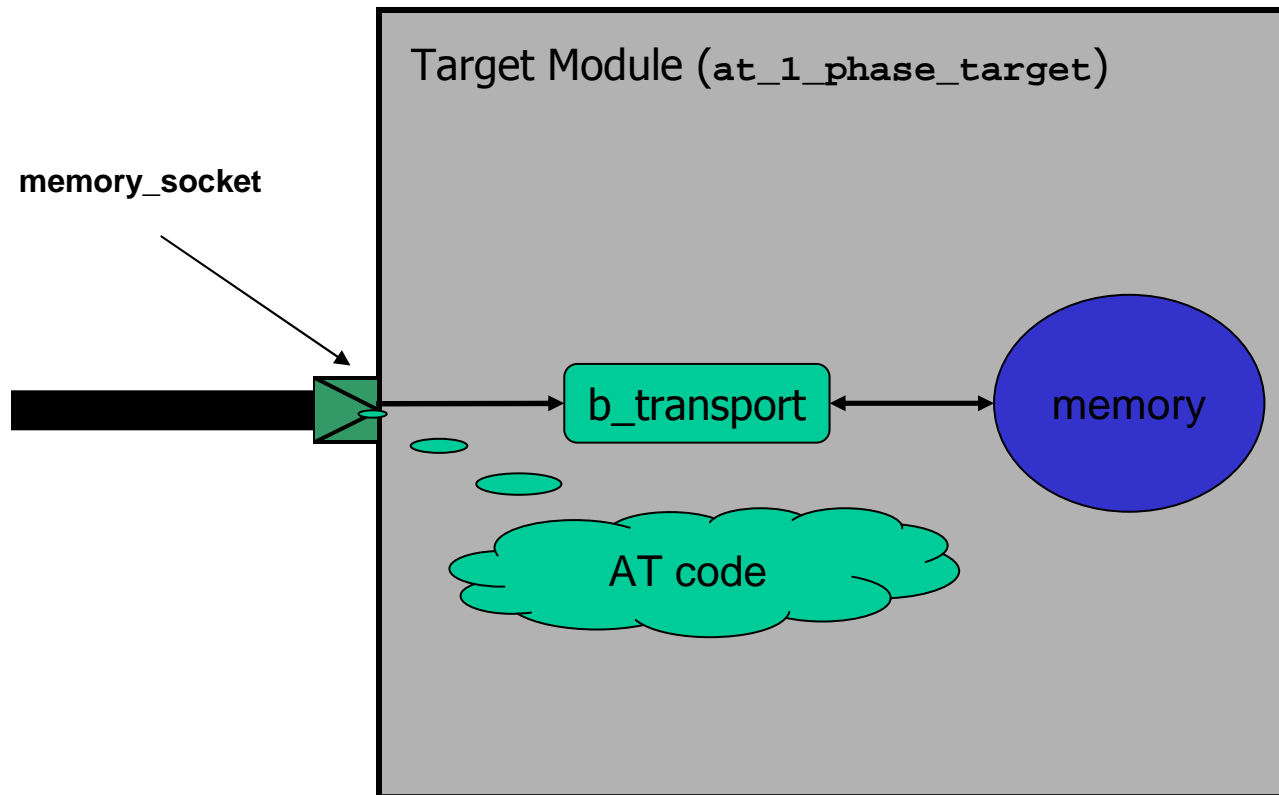
TLM Interface Module



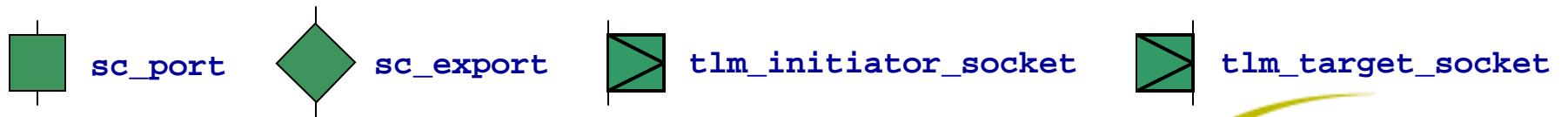
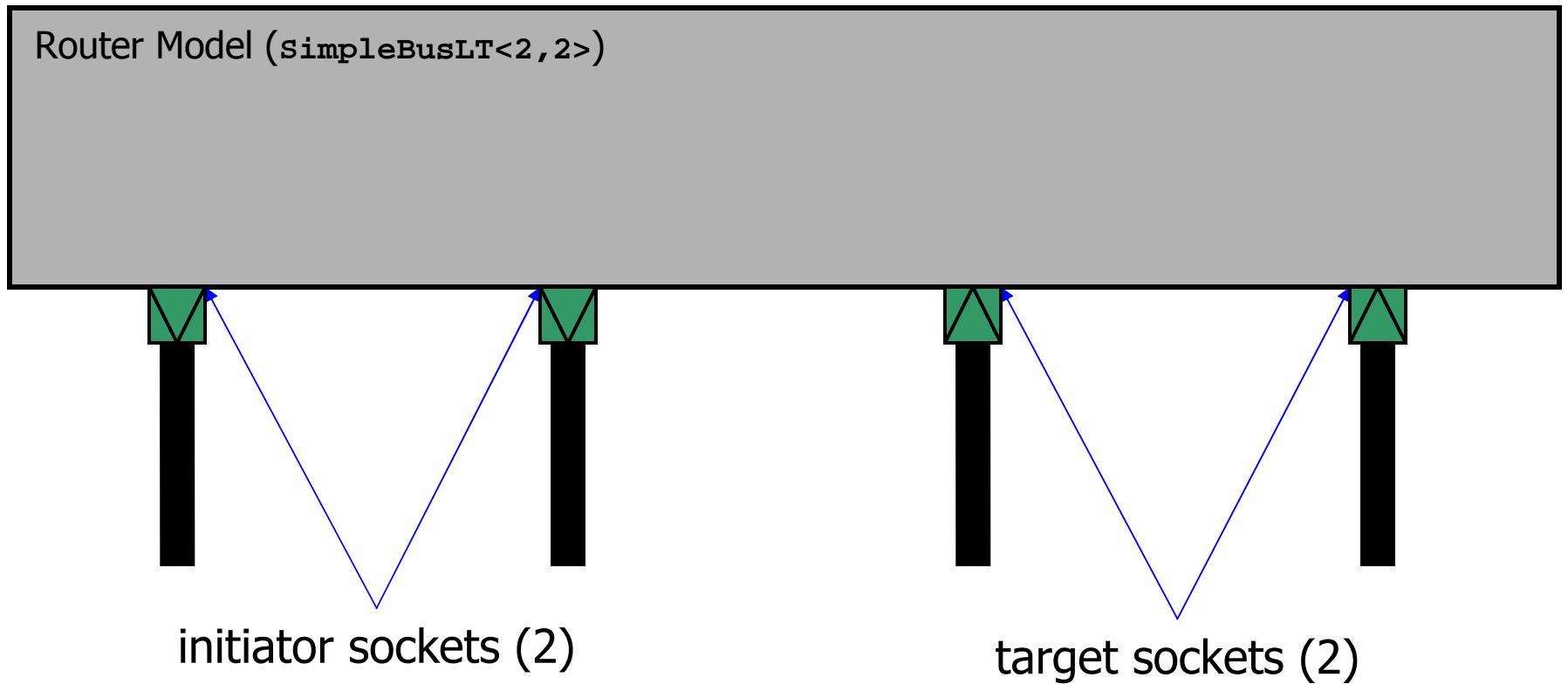
Target Module (lt_target)



Target Module (at_1_phase_target)



Router Component



Expected Timing

